

Data processing by FPGA chip-based SPA method

Ultrasonic testing is widely used in non-destructive testing due to its safety and versatility. Advanced Phased Array systems with high speed scanning have become promising for 3D object imaging.

A phased array system is a multi-channel ultrasonic system, which uses the principle of time-delayed triggering of the transducer transmitting elements combined with time corrected receiving of the detected signals. The main advantage of phased array systems is their ability to vary the angle of insonification in the tested object (sound beam sweeping and focusing) [1].

One of the most common imaging techniques for the object control is SAFT (synthetic aperture focusing technique). This method is based on creation a focused acoustic field for each control point of the object. The disadvantage of SAFT is long duration of image reconstruction.

SPA technique is currently used to solve a large number of NDT problems.

An advanced SPA (Sampling phased array) technology was developed in the Fraunhofer Institute for Non-Destructive Testing (IZFP). SPA allows obtaining sufficient reconstruction of defects at high inspection speeds and inspection of anisotropic materials. The method implies alternate initiation of the array elements and parallel receiving of the reflected signal by all the array elements.

The received ultrasonic signals for each transducer array for each position are saved. Subsequently, they are used as baseline data for imaging of the area under control.

In the first tact of array operation, the first transducer is excited, and then all elements of the array start receiving the reflected signal. The resulting A-scans are stored in memory for subsequent processing. In the second tact, the second array element is excited, and all the arrays receive the reflected signals. This process continues until all the elements of the array have been enumerated.

After saving A-scans for all combinations of the source/receiver, imaging starts. According to the calculated signal propagation time to each of the object points, the required amplitudes are sampled, from which the resulting amplitude of the point is obtained.

High demands to data processing speed make it necessary to perform many operations simultaneously.

Concurrent use of several high-performance processors or the use of the programmable logic matrix allows embodying streaming data from the sensor array.

Using FPGA, several channels are organized. All channels perform the same actions simultaneously. This is done to increase the processing speed. The number of channels is determined by the number of the elements in the array.

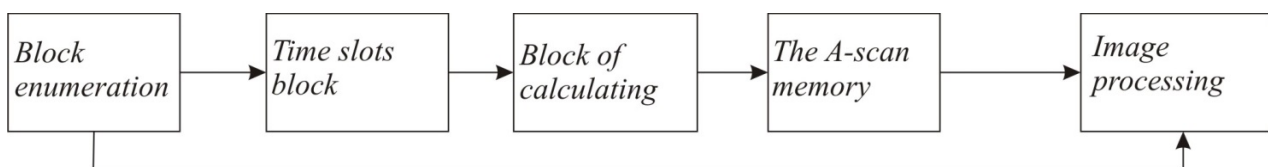


Fig. 1. Block diagram of the data processing channel

To increase the device operation speed, time intervals are calculated before processing. In its memory, FPGA stores only the calculated results, which are required to construct the object image.

The Block enumeration is responsible for determining the estimated number of the current point.

The Time slots block is a memory which stores the ultrasonic propagation time to each point of the tested object.

The Calculation block calculates the required addresses for the A-scan memory.
The A-scan memory stores the digitized signal reflected from the control object.
The Image processing block produces reconstruction of object control image, and *information transmission block* is used to send the results to the display device.

The circuit for 4 channels without image-processing unit will be as follows:

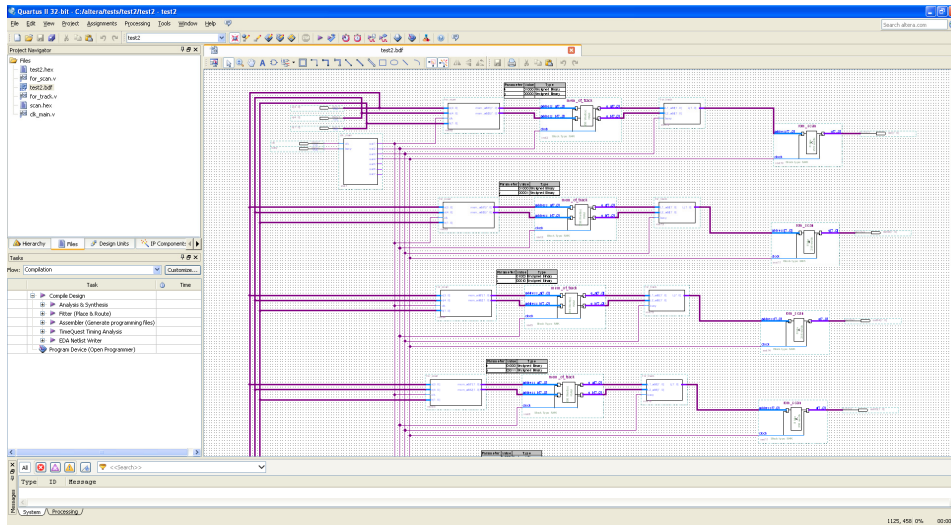


Fig. 2. Circuit realization of SPA on FPGA chip

The problem to be currently solved is minimization of the information processing algorithm for the SPA method. Increase of the processing speed, an acceptable complexity of the process and its cost are new challenges for scientists.

References

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2. K.G. Kvasnikov, A.I. Soldatov, I.O. Bolotina, K.M. Krening, and A.A. Potapenko. The use of geometrical acoustics for the solution of visualization problems. *Russ. J. Nondestruct. Test.*, Vol. 49, No. 11, P. 625–630, Feb. 2014.

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