new technologies and soon domestic units will completely replace foreign units in our hospitals.

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ORGANIZATION OF THE MULTIPORT MEMORY AND COMMUNICATION INTERFACE USING THE FPGA

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The purpose of the research is to determine the time parameters of multiport memory modules based on FPGA and to estimate utilization internal crystal resources. This information can help for future FPGA-based devices developing.

The topic of this work is very important and actual because realization of digital devices based on FPGA is a very perspective line of modern electronics development. There are some advantages of FPGAs. In spite of the young age of the technology FPGAs are now available for product designers. Prices on FPGA are decreasing and the level of circuit integration is increasing. FPGA manufactures produce a wide range of chips with different configuration, level of integration and ip-cores, so the developers of the electronic device can make a choice of FPGA with better parameters. FPGAs represent universal element base [1].

Application of the multiport memory accelerates exchanging of information and improves the overall system performance [2], however, the implementation of multiport memory blocks based on the FPGA causes the following problems:

- Requiring a large number of logic gates on a chip for the project
- Time delays due to using of a large number of crystal elements

Using a large number of logical blocks is necessary for each additional output port which includes "latches" needed to fix the data [3]. The "trace" of the project on the chip is carried out automatically on the basis of optimizing the links between the logic elements. "Tracing" of projects including a huge number of logic elements is impossible to perform to completely eliminate the occurrence of time delays.

Any development of the device, organized by the FPGA, involves the creation of the behavior model, because it is necessary to make a logic description and to create a program code.

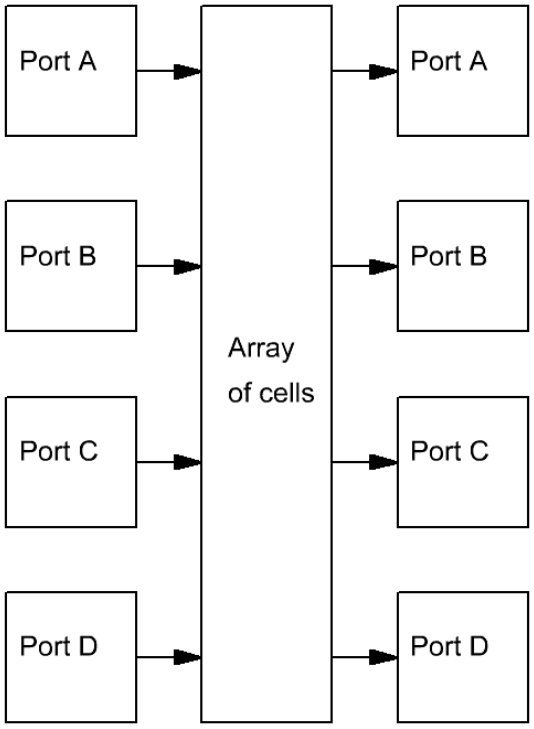

Figure 1. Functional diagram of multiport memory

The basis of any storage device is an array of cells. In RAM memory devices access to a specific cell is provided by using the address decoder. Typically, the output data are latched by the output latch register. There are many variations of input and output ports. Generally, multiport memory

means that a memory device has two or more ports for recording or reading data. The memory block shown in Figure 1 has four ports for writing data and for ports to read data. The direction of the data flow is indicated by arrows in the diagram.

Memory blocks used for this project have one port for data recording and 2 ports (4 ports in case of realization of a multiprocessor system) for reading. All actions of the module are associated with the rising edge of the clock signal. All actions of the module are connected with the event of the rising edge of the clock signal. If the rising edge of clock signal is detected, the signal WE will be checked. If the WE signal is active, i.e. a request to write data is received, the data from the input port will be entered in the array cell. The data reading is performed after writing and output registers hold the data, so a data set for all output ports occurs simultaneously. The algorithm of the memory blocks is shown in Figure 2.

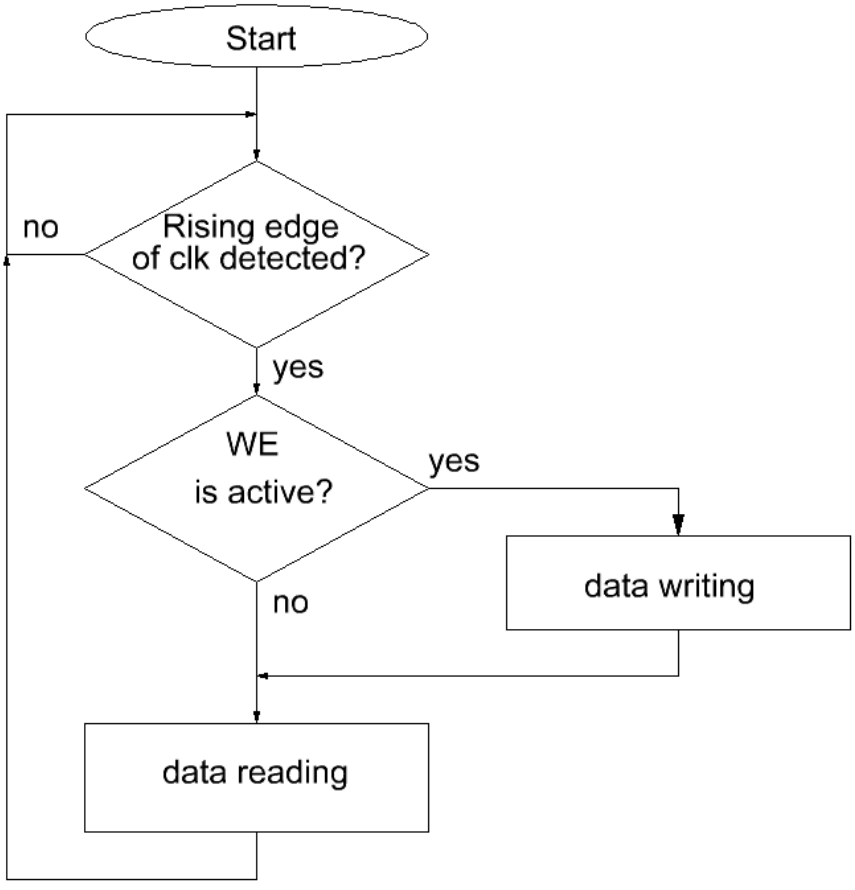

Figure 2. Algorithm of multiport memory

Behavioral models of functional blocks with a different configuration of ports and different amount of data were created to estimate the feasibility of realization multiport memory modules implemented on FPGA systems with multi-threaded processing of information. The timing parameters of the memory blocks were examined by CAD tools, Quartus II. Application of this computer aided design allows accurately reproduce the behavior of real FPGA logic blocks based on the propagation delay of signals. The hardware debugging environment used for this project is kit Cyclone II FPGA Starter Development Board [1].

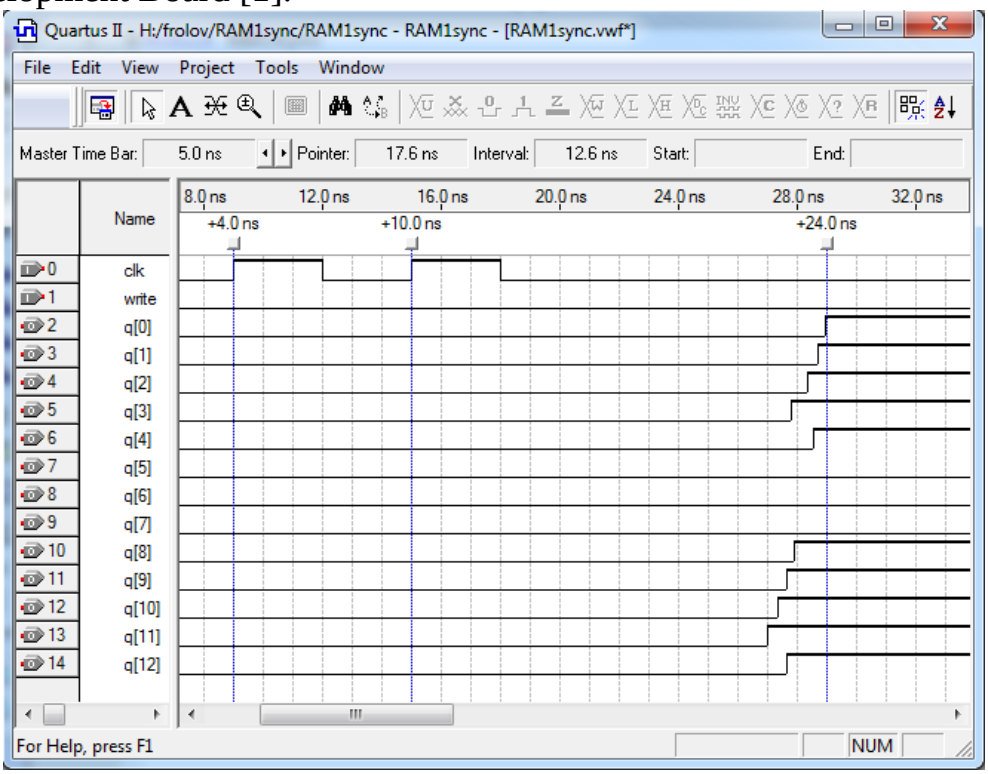

Figure 3. Data reading of the 2 ports memory module

Data[0] – Data[15] are input ports of data,
clk is clock signal,
write is write enable signal,
q[0] – q[15] are output ports of data.

The time diagram shown in the figures shows that time delays increase slightly.

The crystal compile information reports of all the modules projects were saved and performed to compare the effective utilization of resources.

The obtained results clearly show the extent of the use of internal resources of FPGA chip.

Basing on the stored reports, we can conclude that increasing of lines of the output ports significantly increases utilization of the crystal that can cause some difficulties during the design of complex system-on-chip.

Table 1. Comparison of memory block characteristics.

Type of memory block	Number of elements used for projects	Utilization of crystal resources	Data set time	Number of output lines
2 ports	16384	7 %	14 ns	54
3 ports	32768	14 %	16 ns	80
4 ports	65536	27 %	16 ns	132

The research shows that increasing the number of output data ports significantly increases the volume of the internal resources of the FPGA, thus deteriorating the performance of the module slightly. These multiport memory modules can be used in applications requiring high-speed processing and transmission of large amounts of data, such as data collection systems with a large number of sensors and image processing, as delays do not exceed 16 ns. It was also observed that increasing the number of ports also produces increasing data set up time. Increasing the number of output ports produces a more complex project, so a number of logic elements raises, and the total project area is extended. This makes it possible to conclude that with the increasing of the project complexity the length of connections between the logic elements is also increased, hence, the time delays are also increased.

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