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Institute of Non-Destructive Testing  
Department of Industrial and Medical Electronics  
Specialization of Electronics Devices and Facilities

**Master Degree Thesis**

<b>R &amp; D</b>
<i>Research of Power Supply for Capacitor Storage Device</i>

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## ABSTRACT

Nowadays, the technology and research in power supply is widely developed and applied in the power electronics area. This is a comprehensive study of power supply for capacitor storage device by graduate student at Tomsk Polytechnic University who is in the very final stages of completing the master's degree. In this thesis, the general idea of the design of the power supply circuit, the selection of the components and the analysis of the voltage and current of some main blocks will be demonstrated. And the result of my research in the laboratory will also be illustrated later.

The power supply system consists of three blocks, controller, driver and power stage. This device can modify the value and waveform of DC voltage, which means the duty cycle of PWM signal produced from controller can lead the corresponding changes of discharge of capacitor in output circuit in frequency, voltage, rising time and so forth.

The converter features 500W output power, 1kV maximum voltage across the primary storage, 10kHz discharge repetition rate, and 2000 $\mu$ F storage capacitance.

**Keywords:** power electronics, power supply, controller, driver, power stage, PWM, converter.

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# CHAPTER 1: INTRODUCTION

Nowadays, the technology of power electronics has achieved a lot of development and power supply is also widely applied. In this chapter, the general idea of power electronics and the form of power supply will be illustrated.

## 1.1 What is power electronics

Power electronics as a subject usually treated to be the application of solid-state electronics to convert and control the electric power, also referring the research in control, design, integration and computation of time-varying, nonlinear energy-processing electronic system with fast dynamics related to electronic and electrical engineering. Basically, processing and controlling the flow of electric energy by supplying voltages and currents in a form that is optimally suited for user loads is the main aim of power electronics.

The name of power electronics came out in 1960s later than thyristor. In 1974, William E. Newell described the interdisciplinary nature of power

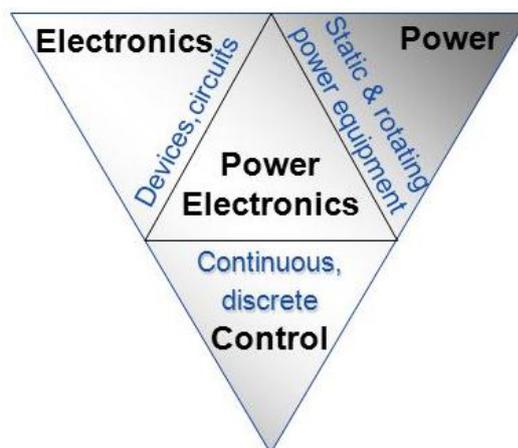


Fig.1.1 William E. Newell's description of power electronics

electronics in the interface between electronics and power with the inverted triangle shown in figure.1.1.

Also, power electronics is currently the most active discipline in electric power engineering worldwide which includes multiple disciplines, such as circuit theory, electric machines, power systems, electromagnetics, solid state physics, electronics, systems and control theory, signal processing, simulation and computing and so on.

Looking back history, the research and development of electronics device such as thyristor had a close relationship with that of power electronics. In 1902, Peter Cooper Hewitt invented the mercury arc rectifier to convert alternating current into direct current, which starting the development of power electronics. But until 1956 the first silicon controlled rectifier (SCR) introduced by General

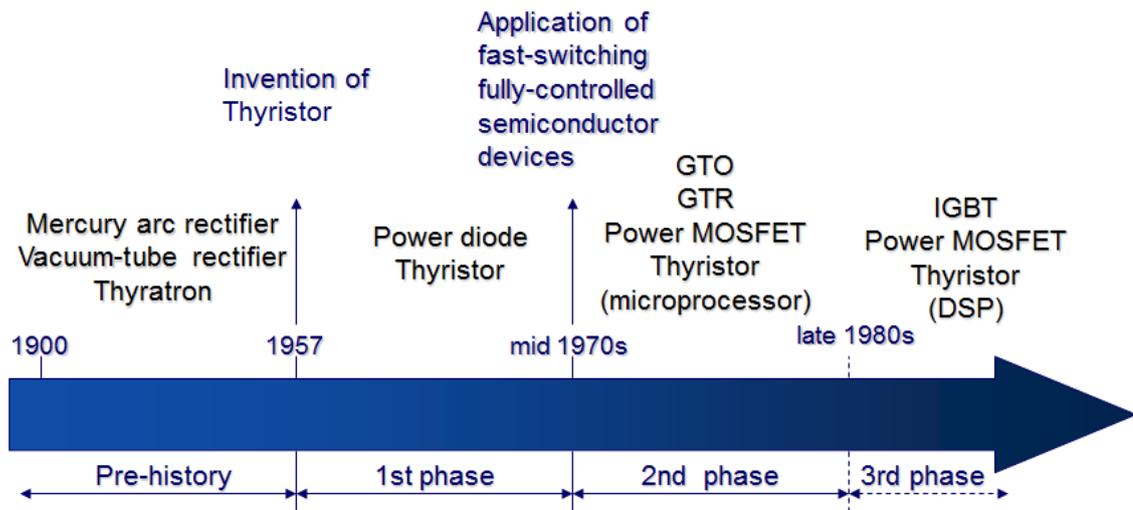


Fig 1.2 The history of power electronics

Electric was treated to be the true beginning of power electronics. Later, the promotion of bipolar junction transistors, power MOSFETs and insulated Gate Bipolar Transistor (IGBT) came out in order. Through the figure 1.2, it can be found that thread of history of the power electronics follows and matched the break-through and evolution of power electronic devices precisely.

The technology of power electronics can be applied in a large number of areas,

e.g. industries, transportation, utility systems, power supplies for all kinds of electronic equipment, residential and home appliances, space technology and other applications.

## 1.2 Power supply

Power supply is one of applications in power electronics, whose range of power scale can change from milliwatts to gigawatts. The aim of the power supply device is to convert and control the electric power.

Both DC and AC electric power can be modified by electric power converter, namely, power converter, converter, switching converter, power electronic circuit and power electronic converter. The changeable property in conversion of DC electric power can be magnitude and those of AC source can be frequency, magnitude and number of phases.

The conversion of power electronics usually can be classified into four forms, AC to DC, DC to AC, DC to Dc and AC to AC. The classification of power converters is shown as table 1.1.

Table 1.1 Classification of power converter

Power output Power input	DC	AC
AC	AC to DC converter (Rectifier)	AC to AC converter (Fixed frequency: AC controller Variable frequency: Cycloconverter or frequency converter)
DC	DC to DC converter (Chopper)	DC to AC converter (Inverter)

The task of power supply is to ensure the currents and power consumed by power converters and loads to meet the requirement of electric energy sources. The figure 1.3 illustrates the general structure of power supply system.

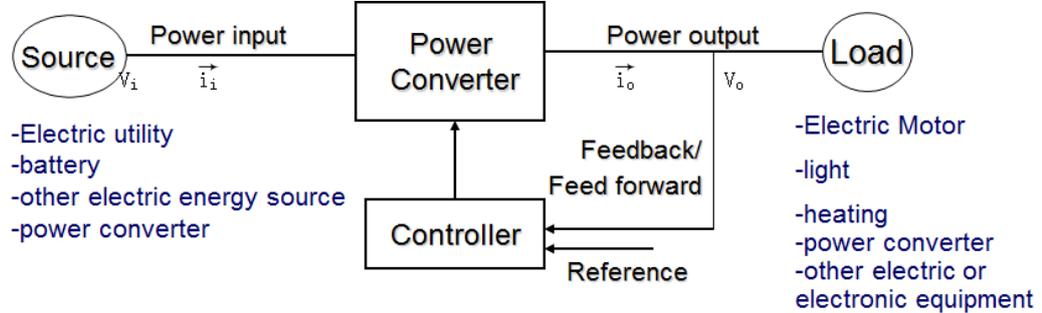


Fig 1.3 Power supply system

The research of power supply for capacitor storage device in this thesis applies DC to DC converter. Where the energy is stored in and released from a magnet field in an inductor or a transformer periodically within a frequency 10MHz. The adjusting of the duty cycle of PWM signal (i.e. the ratio of the on/off times) can easily control the amount of power transferred to the load. Transformer-based converters support the isolation between the input and output source. Generally, the DC-to-DC converter features a switching converter treated to be the heart of switched-mode power supply. There are many topologies to illustrate such circuits. The table 1.2 shows the most common ones.

Table 1.2 The classification of DC-to DC converter

	Forward (energy transfers through the magnetic field)	Flyback (energy is stored in the magnetic field)
No transformer (non-isolated)	Step-down (buck) - The output voltage is lower than the input voltage, and of the same polarity.	Non-inverting: The output voltage is the same polarity as the input.

		<p>Step-up (boost) - The output voltage is higher than the input voltage.</p> <p>SEPIC - The output voltage can be lower or higher than the input.</p> <p>Inverting: the output voltage is of the opposite polarity as the input.</p> <p>Inverting (buck-boost).</p> <p>Cuk - Output current is continuous.</p>
		<p>True buck-boost - The output voltage is the same polarity as the input and can be lower or higher.</p>
		<p>Split-pi (boost-buck) - Allows bidirectional voltage conversion with the output voltage the same polarity as the input and can be lower or higher.</p>
<p>With transformer (isolatable)</p>	<p>Forward - 1 or 2 transistor drive.</p> <p>Push-pull (half bridge) - 2 transistors drive.</p> <p>Full bridge - 4 transistor drive.</p>	<p>Flyback - 1 transistor drive.</p>

In my research, full bridge converter with transformer is applied. The detail information and analysis will be demonstrated later.

Besides the transistors, capacitors also act rather important roles in the circuits. In different topologies, switched capacitor converters depend on the capacitors connected to the input and output alternately. For instance, a switched

capacitor reduces converter to charge two capacitors in series and then discharge them in parallel, which could produce the output power at half the input voltage and twice the current. As they use the discrete quantities of charge operation, such converters also seem to charge pump. They can apply in small currents and also high voltages, because magnetics would break down at such voltages.

There are some terminologies should be concerned including step-down, step- up, continuous current mode, discontinuous current mode, RF noise, input noise and output noise.

## CHAPTER 2: REQUIREMENT & DESIGN

### 2.1 Requirements

Electrical considerations for DC to DC converter power supply system are limited by its application condition. Also the adjustable, precise and stable output voltage signal should be concerned.

The following table 2.1 explains the detail information of output power, input voltage, discharged rate, storage capacitance and so forth.

Table 2.1 Requirements of power supply system

Input voltage	Maximum: 1kV Test: 20V-100V
Output voltage	DC: 3-50V
Load power	1-500W
Discharge repetition rate	10kHz
Storage capacitance	2000 $\mu$ F
Ripple factor, $K_r$	0.5%
Power factor, $\cos\phi$	1
Tolerance $\delta$	<0.5%
Operating condition	Normal
Other conditions	Minimum weight

### 2.2 Design

The general structure can be seen in figure 1.3. The power stage block and controller block including CPU processor and driver should be considered. Also the protected circuits should be added.

### 2.2.1 Power stage

Considering the DC-to-DC converter that converts a source of direct current from one voltage level to another, the transistors, inductors, diodes, capacitors and transforms should be designed very well. Such converters can be divided into two kinds, non-isolation without transformer and isolable one with transformer. And what this thesis discussed is the converter with transformer, whose structure shows as figure 2.1.

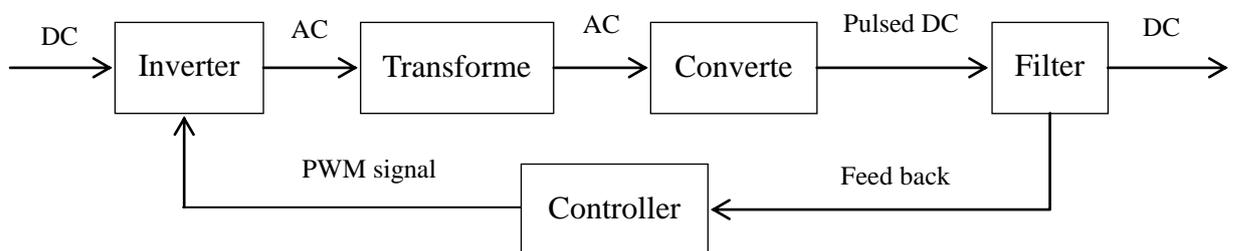


Fig 2.1 The structure of DC-to-DC converter isolated

Compared with non-isolation converter, such system is more complicated but could isolate the input and output, support multiple outputs and change the ratio of input and output. Also, in AC block, the high operation frequency should be applied. Usually, the operation frequency should be better higher than 20kHz that is out of audio whose frequencies capable of being heard by humans to prevent men from the noise made from transformers and inductors.

Concerned to the higher frequency, the full control type transistors such as GTR, MOSFET, and IGBT and so on should be used in the inverter circuit. And the fast recovery diodes should be applied in the converter block.

When it comes to DC-to-DC converter with transformer, such circuits can be classified into the two categories, the single end such as forward and flyback circuits and the double end i.e. half-bridge, full-bridge and push-pull circuit.

The structure of power stage is shown as figure 2.2.

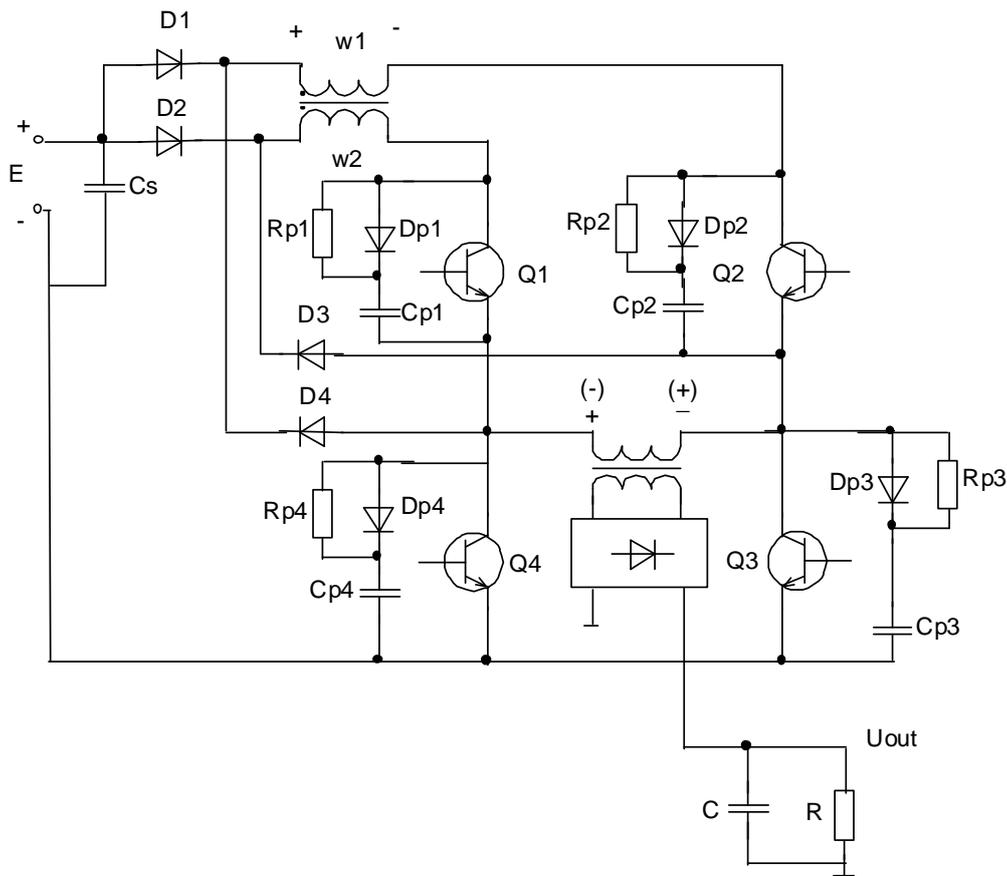


Fig. 2.2 The power stage block

The block applies one capacitor  $C_s$  across the power source, four capacitors  $C_{p1}$ - $C_{p4}$  in the protected circuit and a storage capacitor  $C$  as the load. Four diodes  $D1$ - $D4$ , four diodes  $D_{p1}$ - $D_{p4}$  in the protected circuit and four diodes of the bridge also are placed. Four resistors  $R_{p1}$ - $R_{p4}$  in the protected circuit and the load resistor  $R$  are used. The choke  $Ch$  with two wings and a transformer  $Tr$  are employed. And the four switching full control type transistors  $Q1$ - $Q4$  are also adopts. The following table 2.2 will illustrate the devices and corresponding types used in the power stage block.

Table 2.2 The devices and corresponding types

Symbol	Device	Type	Value
Cs	Capacitor	-	0.33 $\mu$ F
Cp1-Cp4	Capacitor	-	332k $\mu$ F
C	Capacitor	-	2000 $\mu$ F
D1-D4	Diode	КД226Д	-
Dp1-Dp4	Diode	HER208MIC	-
Diodes in the bridge	Diode	HFA16TB	-
Rp1-Rp4	Resistor	ПЭВ25	220 $\Omega$
R	Resistor	-	10 $\Omega$
Q1-Q4	IGBT	G4PF50WD	-
Ch	Choke	Two wings	w1=w2=40
Tr	Transformer	-	w1=w2=40

### Switching transistors

As the power supply system is considered to be the application of the switching of the transistors, the selection of suitable transistors seems very important. Here IGBTs G4PF50WD are chosen to be the switching devices.

Such insulated gate bipolar transistor with ultrafast soft recovery diode features switching loss improve efficiency of all power supply topologies, 50% reduction of  $E_{off}$  parameter, low IGBT conduction losses, tighter parameter distribution coupled with exceptional reliability, industry standard TO-247AC package and optimized for use in welding and switch-mode power supply applications. Lower switching loss allow more cost-effective operation and hence efficient replacement of larger-die MOSFET up to 100kHz, and the diode optimized for performance with IGBTs with minimized recovery characteristics reduce noise, EMI and switching losses. The structure of the IGBT is shown as figure 2.3.

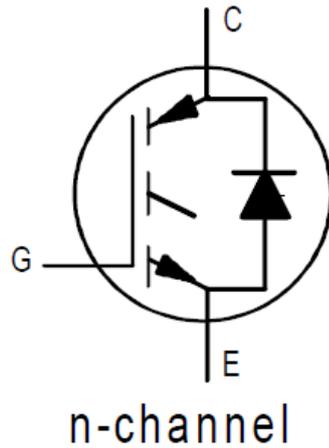


Fig 2.3 The structure of IRG4PF50WD

The following table 2.3 shows the absolute maximum ratings of this transistor.

Table 2.3 The absolute maximum ratings

	Parameter	Max	Units
$V_{CES}$	Collector-to-Emitter Breakdown Voltage	900	V
$I_C @ T_C = 25^\circ\text{C}$	Continuous Collector Current	51	A
$I_C @ T_C = 100^\circ\text{C}$	Continuous Collector Current	28	
$I_{CM}$	Pulsed Collector Current	204	
$I_{LM}$	Clamped Inductive Load Current	204	
$I_F @ T_C = 100^\circ\text{C}$	Diode Continuous Forward Current	16	
$I_{FM}$	Diode Maximum Forward Current	204	
$V_{GE}$	Gate-to-Emitter Voltage	$\pm 20$	V
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	200	W
$P_D @ T_C = 100^\circ\text{C}$	Maximum Power Dissipation	78	
$T_J$ $T_{STG}$	Operating junction and storage temperature range	-50 to +150	$^\circ\text{C}$
	Soldering Temperature, for 10 seconds	300	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1 N •m)	

Here the main idea of maximum parameters of operation are  $V_{CES} = 900V$ ,  $V_{CE(on)typ} = 2.25V$ ,  $V_{GE} = 15V$  and  $I_C = 28A$ . According to the parameters and characters analyzed above, IGBT G4PF50WD can be considered as the optimized switching device.

### **Full-bridge**

The full-bridge circuits compose four transistors as switching devices in the inverter circuit and four diodes in the converter. The upper transistors switch on alternately occupying 50% duty cycle and lower transistors switch on in accordance to the diagonal upper devices but occupying less than 50% duty cycle. When adjusting the duty cycle of lower transistors, the output voltage can be change in corresponding condition. The calculation of the circuit will be demonstrated later.

When the both diagonal transistors switch on, the winding achieves energy from the source with the rising current and when the lower transistor switched off, the winding will release the energy and the current will fall down. Such process can prevent the transformer from the saturation of the magnetic field.

Given the current through the transformer continuous, the following relationship between output voltage and input voltage will exist:

$$\frac{U_o}{U_i} = \frac{2t_{on}}{T} \quad (1 - 1)$$

Where,  $U_o$  is output voltage,  $U_i$  is input voltage,  $t_{on}$  is pulse time and  $T$  is period time. And also the numbers of circle of two windings of transformer are same.

### **Snubber circuit**

Snubber circuit acts to suppress the overvoltage,  $du/dt$ , overcurrent and  $di/dt$  to protect the device from switching loss. The thesis adopts RCD snubber with a small resistor and a diode in series with a small capacitor. Such

combination functions to suppress the dramatic rising voltage across the switching device to prevent the erroneous turn-on of the transistor. Such process is valid because of limiting the rate of rising voltage ( $dV/dt$ ) across the transistor to a value that cannot trigger it. As the voltage across the capacitor is unable to change instantaneously, a decreasing transient current will flow through the capacitor for a moment, which allows the voltage across the transistor to increase more slowly when the transistor switches on. The schematic of RCD snubber is shown as figure 2.4.

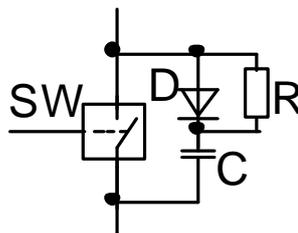


Fig 2.4 RCD snubber schematic

### 2.2.2 Control block

The control block includes the drive circuit and a processor, producing the PWM signals to switch the thyristor of the power supply system.

#### Drive block

As the voltage across the gate and emitter of the thyristor to switch on should reach +15V, the drive block should supply the same voltage. For the easy design, the driver circuit would supply another voltage -15V to switch the device off. The schematic of driver block can be seen in the figure 2.5. The driver circuit should be give voltage +12V to support the system working.

This circuit composes of capacitors, resistors, inductors, transformers, transistors, MOSFETs, self-oscillating half-bridge driver IR2153 and photocouplers TLP250.

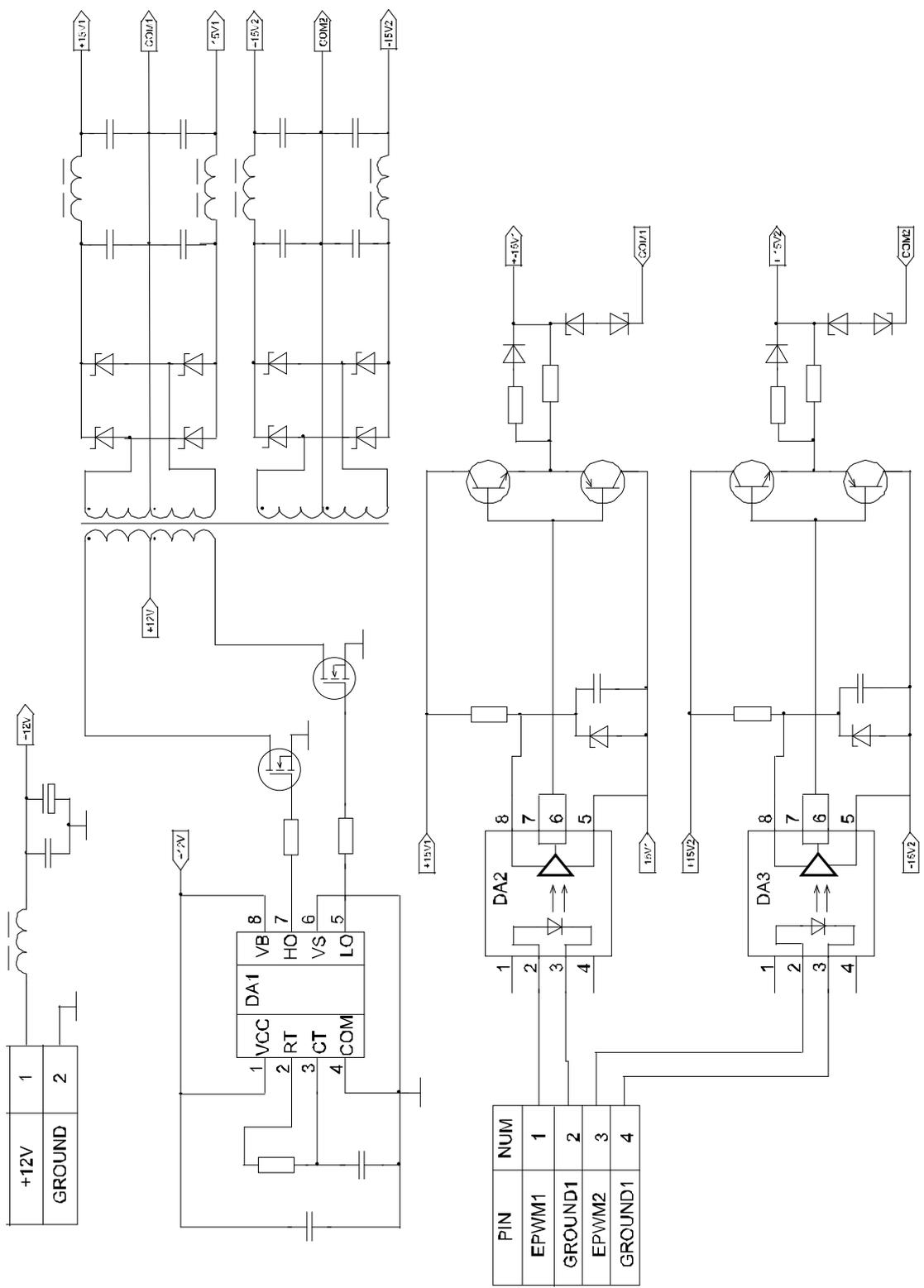


Fig 2.5 Driver block schematic

Where, DA1 represents self-oscillating half-bridge drive IR2153. Its timing diagram of each pin is shown in figure 2.6.

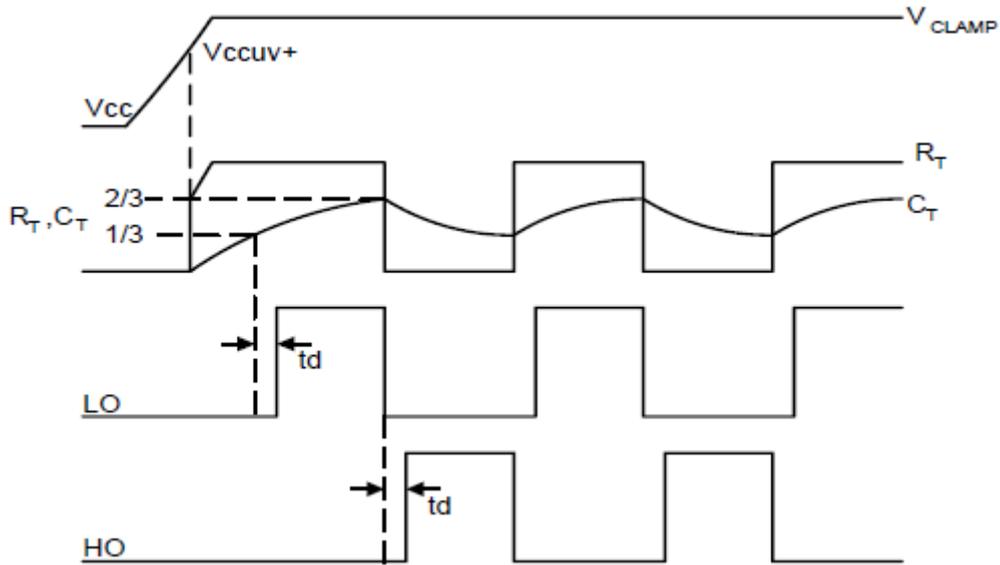


Fig 2.6 Input/output timing diagram of IR2153

The signal produce from pin LO and HO switch on and off the corresponding MOSFETs VT5 and VT6 alternatively.

DA2 represents photocoupler TLP250 that consists of a GaAlAs light emitting diode and an integrated photodetector. The schematic of it is shown as

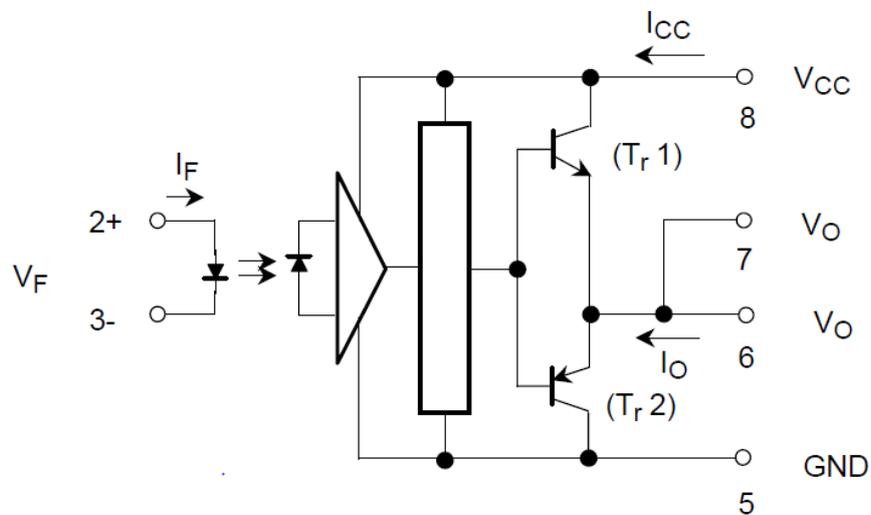


Fig 2.7 TLP250 schematic

figure 2.7.

TLP250 is used for gate driving circuit of IGBT in the pull-push circuit.

The drive block is supplied by +12V DC voltage from power supplier. The voltage will be change up to +15V and -15V after processing through the converter circuit. It supports the photocoupler system with push-pull circuit. The photocoupler is controlled by CPU block that adjusts the pulse time to switch on and off the transistors in pull-push circuit. Finally, the driver block produces +15V and -15V signal to control the power stage system.

### CPU block

The center of the CPU block is digital signal processor (DSP). In this research, DSP TMS320F28335 from Texas Instruments is employed. The features of the processor are shown in table 2.4.

Table 2.4 TMS320F28335 hardware features

Features	F28335(150MHz)
Instruction cycle	6.67ns
Floating-point Unit	Yes
3.3-V on-chip flash (16-bit word)	256K
Single-access RAM (SARAM) (16-bit word)	34K
One-time programmable (OTP) ROM (16-bit word)	1K
Code security for on-chip flash/SARAM/OTP blocks	Yes
Boot ROM (8K x 16)	Yes
16/32-bit External Interface (XINTF)	Yes
6-channel Direct Memory Access (DMA)	Yes
PWM outputs	ePWM 1/2/3/4/5/6
HRPWM channels	ePWM 1A/2A/3A/4A/5A/6A
32-bit Capture inputs or auxiliary PWM outputs	eCAP 1/2/3/4/5/6

32-bit QEP channels (four inputs/channel)	eQEP 1/2
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Table 2.4 TMS320F28335 hardware features (continued)

Watchdog timer		Yes
12-Bit ADC	No. of channels	16
	MSPS	12.5
	Conversion time	80 ns
32-Bit CPU timers		3
Multichannel Buffered Serial Port (McBSP)/SPI		2 (A/B)
Serial Peripheral Interface (SPI)		1
Serial Communications Interface (SCI)		3 (A/B/C)
Enhanced Controller Area Network (eCAN)		2 (A/B)
Inter-Integrated Circuit (I2C)		1
General Purpose I/O pins (shared)		88
External interrupts		8

The controller features high-performance static CMOS technology, high-performance 32-bit CPU, six-channel DMA controller, 16-bit or 32-bit external interface , three 32-bit CPU time, 12-bit ADC with 16 channels, 64 GPIO pins and low-power mode and so on.

The function of the CPU block is to produce the PWM signals that control the driver block. The CPU block also receives the feedback signal from the power stage output. The other schematic of CPU block is shown as figure 2.8.

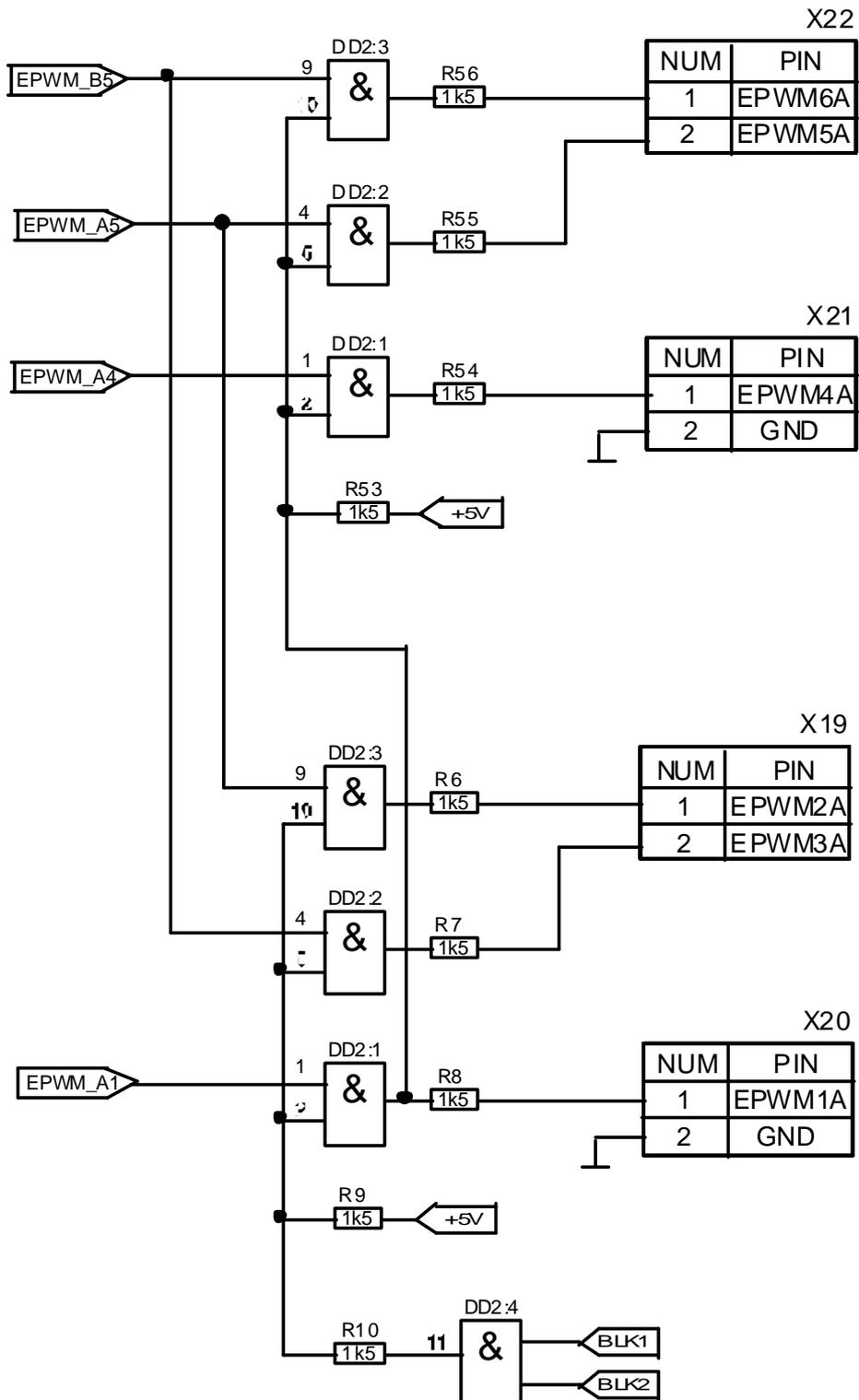


Fig 2.8 CPU block (part 1)

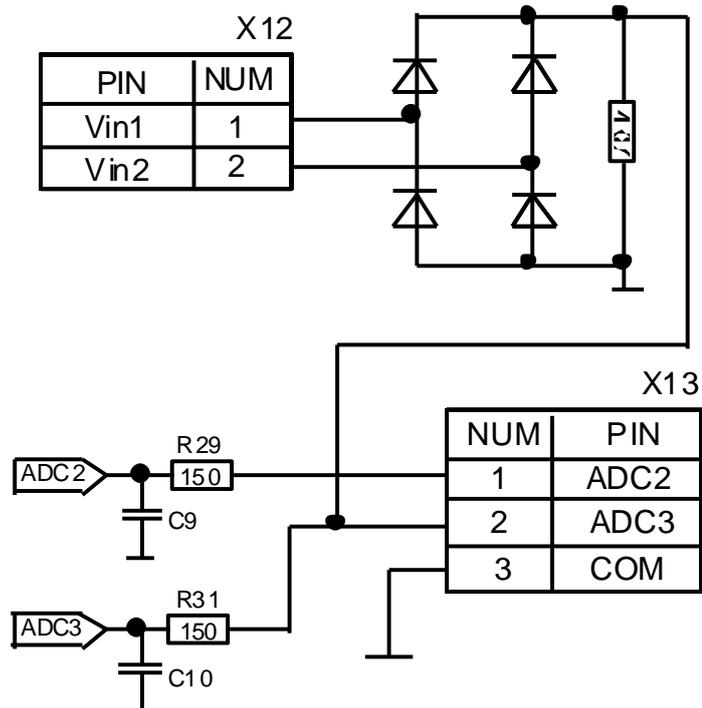


Fig 2.8 CPU block (part 2)

The port EPWM\_A5, EPWMB5 and EPWM A1 in the part 1 of CPU block are generated from processor and the port ADC3 in the part 2 of CPU block receives the feedback signal from power stage.

## CHAPTER 3: ANALYSIS & IMPLEMENTATION

This chapter discusses the process of power stage that is controlled by PWM signals. The inductors and capacitors will perform the action of charging and discharging.

### 3.1 The analysis of current, voltage and energy

As the power stage system is steered by the PWM signals, the inductors and capacitors act to charge and discharge with the direction changed echoing to the transistors' switching on and switching off.

According to figure 2.2, set the timing of EPWM1, EPWM2, EPWM3 and EPWM4 to represent the PWM signals across the gate-to-emitter of Q1, Q2, Q3 and Q4 respectively. The duty cycle of upper switches Q1 and Q2 occupy 50% alternatively. The pulse time of signals to switch on Q3 and Q4 are in accordance with those of Q1 and Q2 but can be divided into several fragments. For the easy analysis, the pulse time of lower switches Q3 and Q4 will not be divided but the duty cycle should be less than 50%. whose diagram is shown in the figure 3.1.

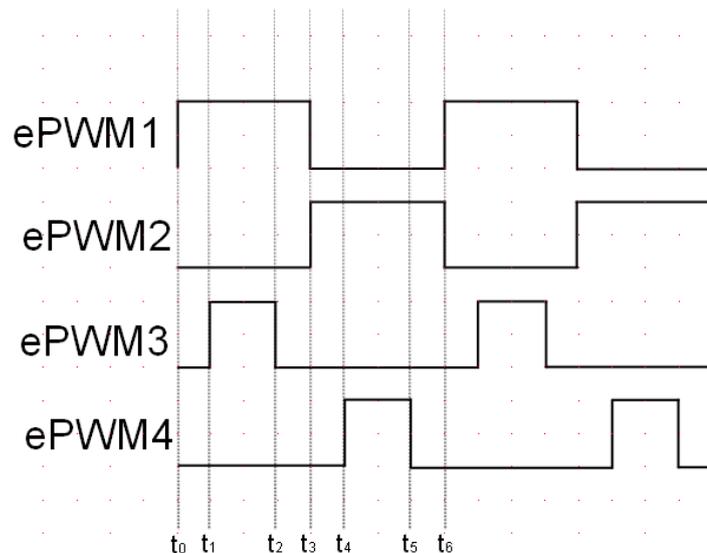


Fig 3.1 The timing of ePWM1, ePWM2, ePWM3 and ePWM4

Where, the period time equals the duration from  $t_0$  to  $t_6$  and the period time is set as  $100\mu\text{s}$ . The method of dividing the timing sequence of switching transistors is illustrated in figure 3.1. The whole period is separated into 6 sections and the current flow condition and the energy transmission in the corresponding section will be discussed.

Section 1 ( $t_1$ - $t_2$ ): At the moment  $t_1$ , transistor Q1 and Q3 are turn on. The DC voltage of source applies to the primary winding of Tr1 and the winding  $w_2$  of the choke. While the polarity of across Tr1 is right positive and left negative. The current flows in this chain: positive terminal of power supply E, diode D2, the winding  $w_2$  of the choke, transistor Q1, transformer Tr1, transistor Q3 and negative terminal of the power supply E. And the value of current is increasing.

The process is called positive charge. Because the windings achieve the energy from source supplier and the current through the loop circuit will increase.

Section 2 ( $t_2$ - $t_3$ ): At the moment  $t_2$ , transistor Q3 is turn off. The polarity across the transformer Tr1 has changed but current through it is going down because the winding releases energy to the circuit. The current flows in this chain: the winding  $w_2$  of choke, transistor Q1, transformer Tr1, and diode D3. This period is called energy recovery since it recovers energy stored in the winding  $w_2$  from previous period to the transformer Tr1. And the polarity across the winding  $w_2$  of choke also changes.

Section 3 ( $t_3$ - $t_4$ ): At the moment  $t_3$ , the transformer Tr1 gets sufficient magnetization. Switches off transistor Q1 while switches on transistor Q2. As the winding  $w_1$  of choke has initial energy from previous period, the energy transmits to loop again and the current flows in this chain: the winding  $w_1$ , transistor Q2, the transformer Tr1 and diode D4. In this case, the polarity of the voltage across the transformer Tr1 is reversed, left positive and right negative. And the magnetic core of the transformer Tr1 starts remagnetizing. The current through transformer

flows in opposite direction compared with the last section but the absolute value decreases.

Section 4 ( $t_4$ - $t_5$ ): At the moment of  $t_4$ , transistor Q4 is switched on. The principle of the performance is same as that of section 1. Both winding of choke and transformer achieve energy from source and the current though them will increase but in the different direction.

Section 5 ( $t_5$ - $t_6$ ): At the moment of  $t_5$ , transistor Q4 is switched off. The process of this period has the same principle as Section 2. The winding of choke releases energy to the loop with transformer. The transformer will get sufficient magnetization but the current will be slow down.

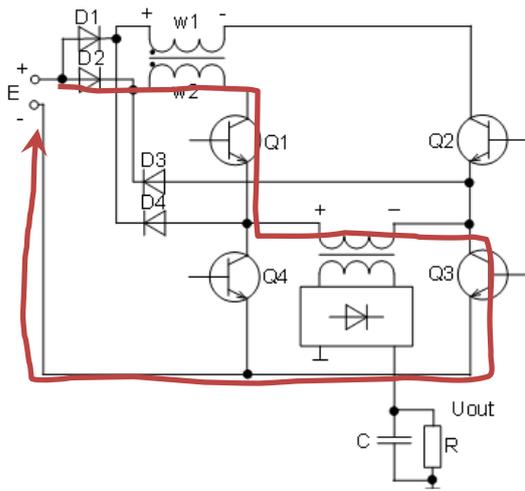
Section 6 ( $t_0$ - $t_1$ ): t the moment of  $t_0$ , transistor Q1 switches on and Q2 switched off. The principle of this period is same as Section 3.

The table 3.1 would describe the whole process of the converter clearly. And the series of diagrams in the figure 3.2 illustrate the current flow condition.

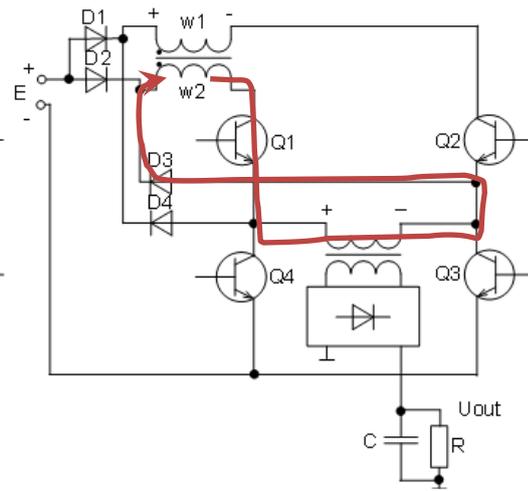
Table 3.1 The process of converter in one period

Period	Description	Path of current	Duration
1	Positive charge (Q1 and Q3 on)	$E \rightarrow D2 \rightarrow w_2 \rightarrow Q1 \rightarrow$ $Tr1 \rightarrow Q3 \rightarrow E$	$t_0 \sim t_1$
2	Recovering energy from $w_2$ to Tr1 (Q1 alone on)	$w_2 \rightarrow Q1 \rightarrow Tr1 \rightarrow D3$ $\rightarrow w_2$	$t_1 \sim t_2$
3	Remagnetization of Tr1 (Q2 alone on)	$w_1 \rightarrow Q2 \rightarrow Tr1 \rightarrow D4$ $\rightarrow w_1$	$t_3 \sim t_4$
4	Positive charge (Q2 and Q4 on)	$E \rightarrow D1 \rightarrow w_1 \rightarrow Q2 \rightarrow$ $Tr1 \rightarrow Q4 \rightarrow E$	$t_4 \sim t_5$
5	Recovering energy from $w_1$ to Tr1 (Q2 alone on)	$w_1 \rightarrow Q2 \rightarrow Tr1 \rightarrow D4$ $\rightarrow w_1$	$t_5 \sim t_6$
6	Remagnetization of Tr1 (Q1 alone on)	$w_2 \rightarrow Q1 \rightarrow Tr1 \rightarrow D3$ $\rightarrow w_2$	$t_0 \sim t_1$

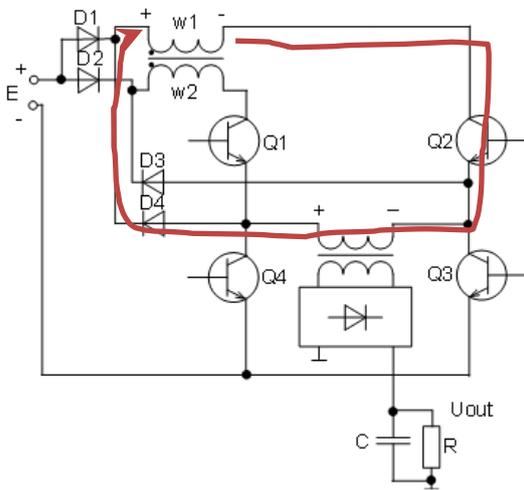
Figure 3.2 Current flows in the section 1 to 6



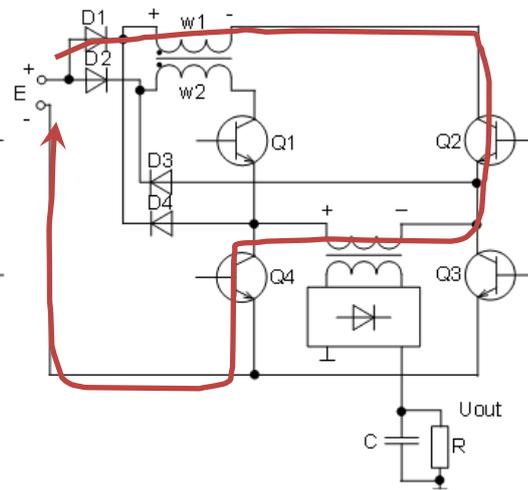
(a) Positive charge. Q1 and Q3 are turn on



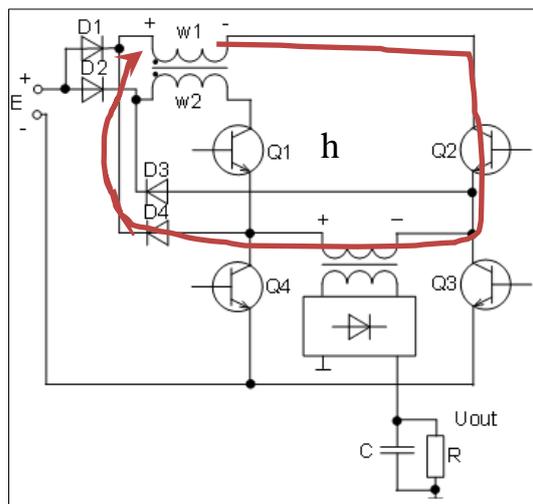
(b) Recovery energy. Q1 alone is turn on



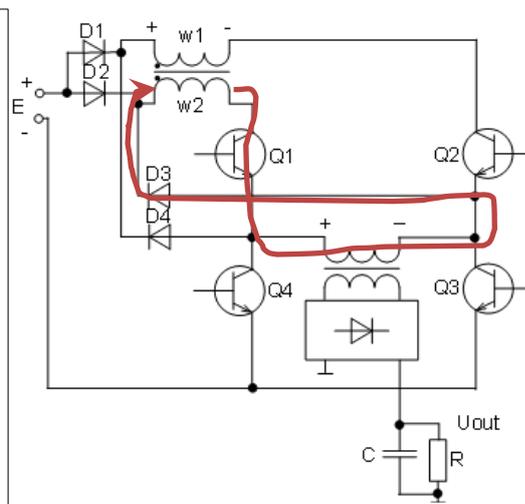
(c) Reverse the polarity and remagnetization, Q2 alone is turn on.



(d) Positive charge. Q2 and Q4 are turn on



(e) Recovering energy. Q2 alone is turn on



(f) Reverse the polarity and remagnetization, Q1 alone is turn on

According to the analysis of the action of current responding with the switches, the waveform of current through one of wings of choke can be easily verified as figure 3.3.

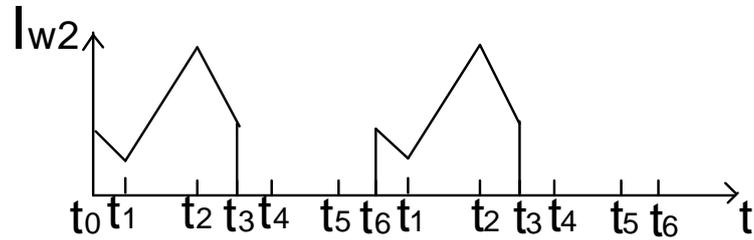


Fig 3.3 Current through wing 2 of the choke

## 3.2 Software

The software for the control block is implemented on digital signal processor in C. It produces the PWM signals, sampling the electric signals from output as feedback. Details about the idea to program the signals and feedback system will be described.

### 3.2.1 PWM

In the figure 2.8 CPU block, it can be clear to be found that ports EPWM\_A5, EPWM\_B5 and EPWM\_A1 can produce PWM signals ePWM1 to 4 and port Vin1 and Vin2 can sample the voltage information to the ADC block.

The duty cycle of ePWM1 and ePWM2 should be set as 50% alternatively and that of ePWM3 and ePWM4 should be less than 50% following ePWM1 and ePWM2 respectively. As the operation frequency is 10kHz, the time  $t_0$  to  $t_6$  in the figure 3.1 the timing of ePWM1, ePWM2, ePWM3 and ePWM4 could be set like such:

$t_0 = 0$ , beginning of a period;

$t_2 - t_1 = 33\mu\text{s}$ , pulse width of ePWM3;

$t_3 - t_0 = 50\mu\text{s}$ , pulse width of ePWM1;

$t_5 - t_4 = 33\mu\text{s}$ , pulse width of ePWM4;

$t_6 - t_3 = 50\mu\text{s}$ , pulse width of ePWM2;

$t_6 = 100\mu\text{s}$ , end of a period;

$\Delta t$  represents the interval of other is 8~9  $\mu\text{s}$ .

The logic diagram of PWM signals according to the CPU block can be simplified to the figure 3.4.

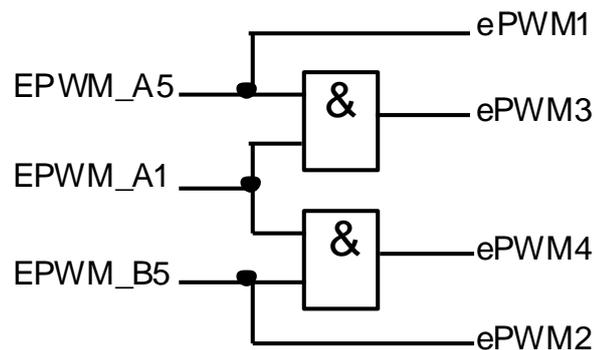


Fig 3.4 the logic of PWM signals

So, the waveforms of EPWM\_A5 and EPWM\_B5 can be set same as those of ePWM1 and ePWM2 respectively. And the EPWM\_A1 just combines the waveforms of ePWM3 and ePWM4. Finally, the waveforms of EPWM\_A5 and EPWM\_B5 and EPWM\_A1 can be illustrated as figure 3.5.

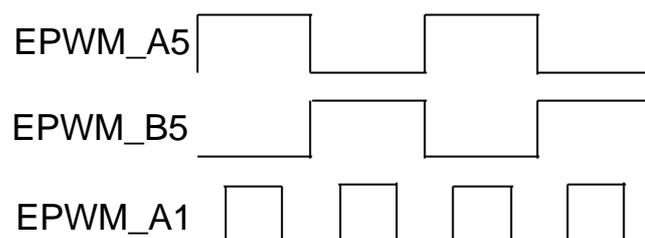


Fig 3.5 The timing of EPWM\_A5 and EPWM\_B5 and EPWM\_A1

Where, the operation frequency is 10kHz, meaning the 100 $\mu\text{s}$  period time. And considering the duty cycle, the program to set the EPWM\_A5, EPWM\_B5 and EPWM\_A1 is written as following:

```

// upper EPWM_A5 and EPWM_B5
//TB
EPwm5Regs.TBPRD = 3750; //Set period time 100µs
EPwm5Regs.TBPHS.half.TBPHS = 0; // Set Phase register to zero
EPwm5Regs.TBCTL.bit.CTRMODE = 2; // Symmetrical mode
EPwm5Regs.TBCTL.bit.PHSEN = TB_DISABLE; // Master module
EPwm5Regs.TBCTL.bit.PRDLN = TB_SHADOW; //shadow mode
EPwm5Regs.TBCTL.bit.SYNCSEL = TB_CTR_ZERO; //Sync down-stream
module
//CC
EPwm5Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW; //shadow mode
enable
EPwm5Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
EPwm5Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on
CTR=Zero
EPwm5Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on
CTR=Zero
//AQ
EPwm5Regs.AQCTLA.bit.CAU = AQ_CLEAR; // set actions for EPWM_A5
EPwm5Regs.AQCTLA.bit.CAD = AQ_SET;
EPwm5Regs.AQCTLB.bit.CBU = AQ_SET; //set action for EPWM_B5
EPwm5Regs.AQCTLB.bit.CBD = AQ_CLEAR;
//DB
EPwm5Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; // enable
Dead-band module
EPwm5Regs.DBCTL.bit.POLSEL = 0; //DB_ACTV_HIC; // Active Hi
complementary
EPwm5Regs.DBCTL.bit.IN_MODE = 2;

```

```

EPwm5Regs.DBFED = 0; // FED = 0 TBCLKs
EPwm5Regs.DBRED = 0; // RED = 0 TBCLKs

EPwm5Regs.CMPA.half.CMPA = 1875; //duty cycle 50%, pulse width 50µs
EPwm5Regs.CMPB = 1875; //duty cycle 50%, pulse width 50µs

//lower EPWM_A1
//TB
EPwm1Regs.TBPRD = 625; //set period time 16.67µs
EPwm1Regs.TBPHS.half.TBPHS = 625; //Set Phase register to 625
EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; //
Symmetrical mode
EPwm1Regs.TBCTL.bit.PHSEN = TB_ENABLE; // Slave module
EPwm1Regs.TBCTL.bit.PHSDIR = TB_DOWN;
EPwm1Regs.TBCTL.bit.PRDLT = TB_SHADOW; //shadow mode
EPwm1Regs.TBCTL.bit.SYNCSEL = TB_SYNC_IN; // sync flow-through
//CC
EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW; //Shadow mode
EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on
CTR=Zero
EPwm1Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on
CTR=Zero
//AQ
EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR; // set actions for EPWM_A1
EPwm1Regs.AQCTLA.bit.CAD = AQ_SET;
//DB
EPwm1Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; // enable

```

Dead-band module

```
EPwm1Regs.DBCTL.bit.POLSEL = 0; //DB_ACTV_HIC; // Active Hi  
complementary
```

```
EPwm1Regs.DBCTL.bit.IN_MODE = 2;
```

```
EPwm1Regs.DBFED = 0; // FED = 0 TBCLKs
```

```
EPwm1Regs.DBRED = 0; // RED = 0 TBCLKs
```

In the PWM program, what the data need to be changed is TBPRD to change the period time and CPMA or CMPB to adjust the duty cycle. The table 3.2 lists the parameters of chip and output PWM signals.

Table 3.2 Table.1 The information of EPWM signals supplied by microcontroller

	TBPRD	CMP	Period ( $\mu$ s)	Pulse width ( $\mu$ s)	Duty cycle (%)	Output voltage (V)
ePWM1	3750	1875(A5)	100	50	50	5
ePWM2	3750	1875(B5)	100	50	50	5
ePWM3	3750	1250(A1)	100	33.33	33.33	5
ePWM4	3750	1250(A1)	100	33.33	33.33	5

### 3.2.2 Feedback

To get a stable output voltage from power stage, the pulse width of lower transistors should be changed in respond. So the feedback system is necessary to be added to the CPU block system.

The schematic of feedback system is shown as figure 3.6.

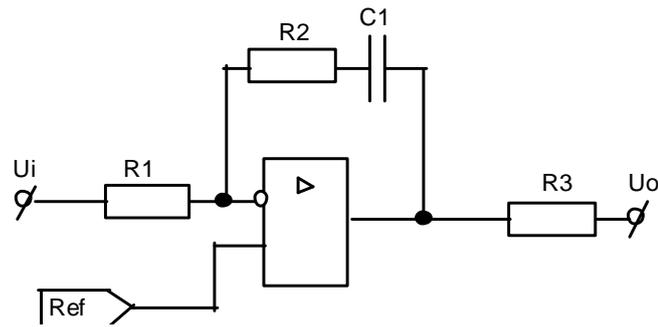


Fig 3.6 Feedback schematic

The program of feedback can be written like this:

```

Err = ref - Adc_result ;
Xn = Err * (Ki + Kp) + Err1 * (Ki - Kp);
Err1 = Err;
b += Xn;
EPwm1Regs.CMPA.half.CMPA = (Uint16) b;

```

Where, Adc\_result is a digital value converted from the voltage value achieved from output of power stage. The ref means the reference value of CMPA of EPWM1. Ki and Kp represent integral and proportional coefficient respectively. The value of b access to CMPA of EPWM1 will be adjusted by the feedback signal to change the duty cycle of lower transistors to produce a stable voltage.

## CHAPTER 4: EXPERIMENT

After the analyzing the power stage and composing the program, the next step in the power supply is with an experiment. The process is listed as the follow:

1. Connect the DSP to laptop;
2. Set the frequency of ePWM signals as 10kHz, the duty of ePWM1 and ePWM2 as 50% and the duty of ePWM3 and ePWM4 as 33.33% respectively.
3. Compile the program and download it;
4. Burn on load part, two resistors ( $18\Omega \pm 10\%$ , ПЭВ-50X-70) and two series capacitors (1000 $\mu$ F, 100V) in parallel.
5. Then connect the pins of ePWM of processor to the corresponding ports of the target circuit. Check the junction again;
6. Supply +13V DC voltage on drive block and +20V DC voltage on the DC-DC converter;
7. Switch on the power, probe and achieve the data of each component need;
8. Keep the duties of ePWM3 and ePWM4 as 33.33% and change the input voltage, then probe and achieve all the data of components wanted;
9. Keep the input voltage as 40V and change the duties of ePWM3 and ePWM4, then probe achieve the corresponding data;
10. Get conclusion.

### 4.1 Some important waveforms

The waveforms of the electric signals of some devices such as choke, thyristors, transformers and capacitor can unveil the characteristics and function of the power supply system.

#### 4.1.1 The voltage across the gate-to-emitter of the IGBT

The waveforms of ePWM1, ePWM2, ePWM3 and ePWM4 to drive the corresponding transistors Q1, Q2, Q3 and Q4 are shown as figure 4.1.

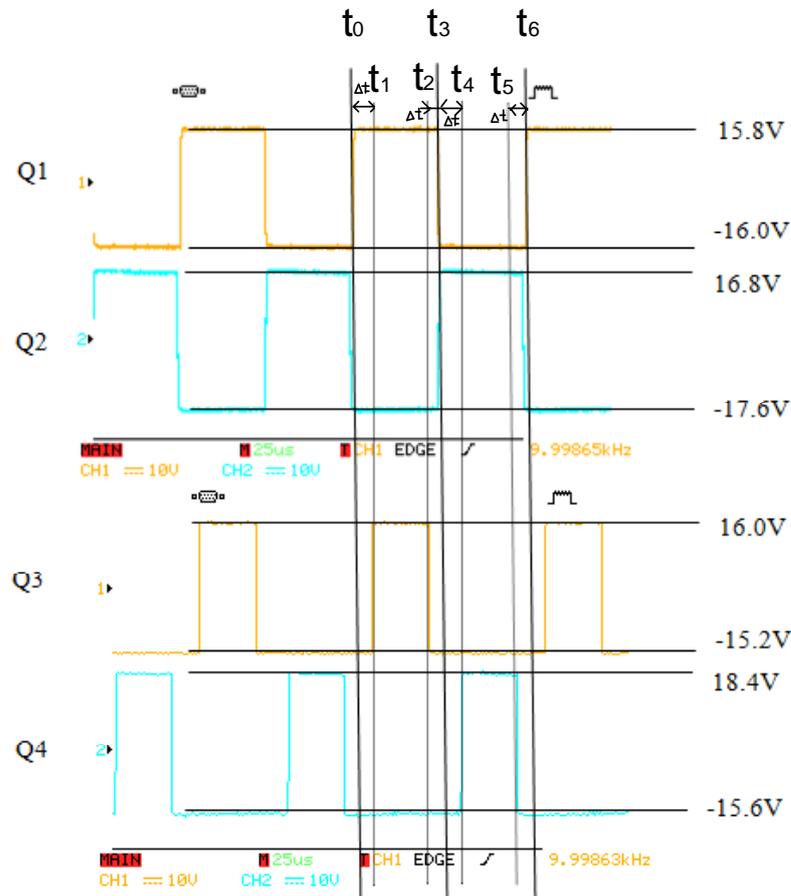


Fig 4.1 The voltage across the gate-to-emitter of the IGBT

The voltage value general equals to that of control block system, which meets the requirement to switch on and switch off the transistors. The frequency, duty cycle and phase are also according with the design and implement.

#### 4.1.2 The voltage across the collector-to-emitter of the IGBTs and the current through them

To research the voltage across the collector-to-emitter of the switch could be better to find the performance of the device to switch on and switch off.

The figure 4.2 describes the voltage across the collector-to-emitter of the upper transistor Q2 and the current through it.

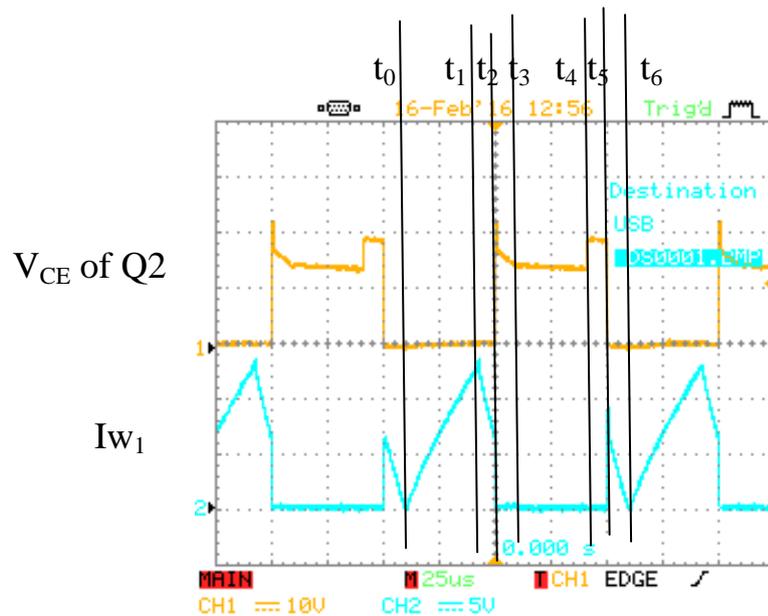


Fig 4.2 The voltage across the collector-to-emitter of O2 and  $I_{w1}$

According to the figure 4.2, it can be found that when the transistor switches on, the current is available while the voltage is close to 0; and when the transistor switches off, the current is close to 0 while the voltage is available. So, the power of switching on and switching off of the transistor seems very less.

When the transistor switches off, the voltage rises up sharply; but thanks to the snubber circuit, the peak value decreases a lot.

The figure 4.3 describes the voltage across the collector-to-emitter of the lower transistor Q4 and the current through the transformer.

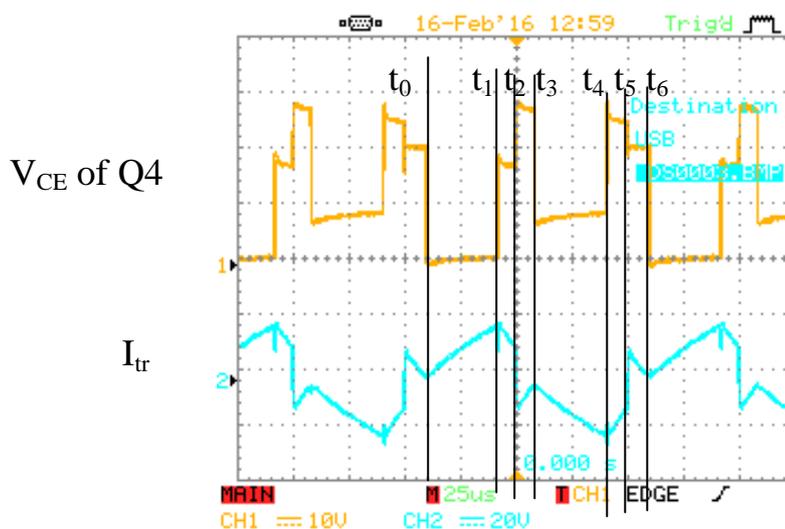


Fig 4.3 the voltage across the collector-to-emitter of Q4 and  $I_{tr}$

### 4.1.3 The voltage across the transformer

The voltage across the transformer actually is inverted and its waveform can decide the final result of output such as ripple, power factor, tolerance and so on. The figure 4.4 shows the waveform of the voltage across the primary windings of the transformer.

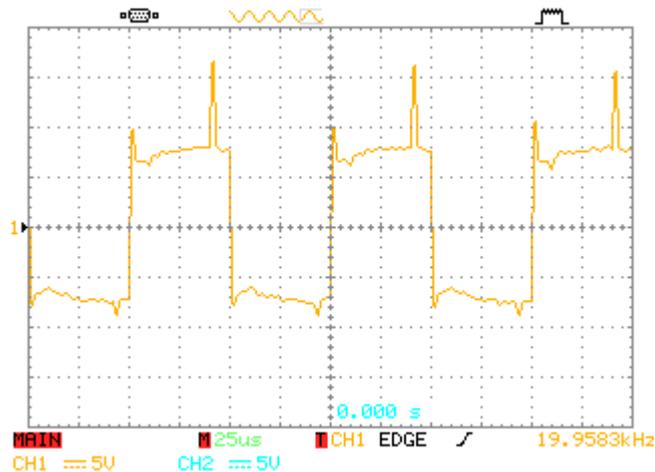


Fig 4.4 The voltage across the transformer

Compared with waveform of primary coil, that of secondary coil seems smoother. As discussed before, transformer-based converters may provide isolation between input and output, which would protect the device and eliminate the noise error. Also it is not difficult found that the switching actions cause the pulse and the higher duty cycle leads the bigger current and higher voltage across the transformer.

## 4.2 The power stage without feedback

### 4.2.1 When the duty cycle is certain, change input voltage

After being changed by a bridge, the DC voltage finally comes out. When input voltage is 20V DC as set at the beginning, the output voltage is 5.39V DC. Change the input DC voltage the corresponding output voltage can be seen as table 4.1. And the relationship between input voltage and output voltage

corresponding to the duty cycle 33.33% is shown as figure 4.5.

Table 4.1 the relationship between input voltage and output voltage  
(duty cycle 33.33%)

Vin(V)	20	25	30	35	40	45
Vout(V)	5.39	6.45	7.27	7.96	8.55	9.04

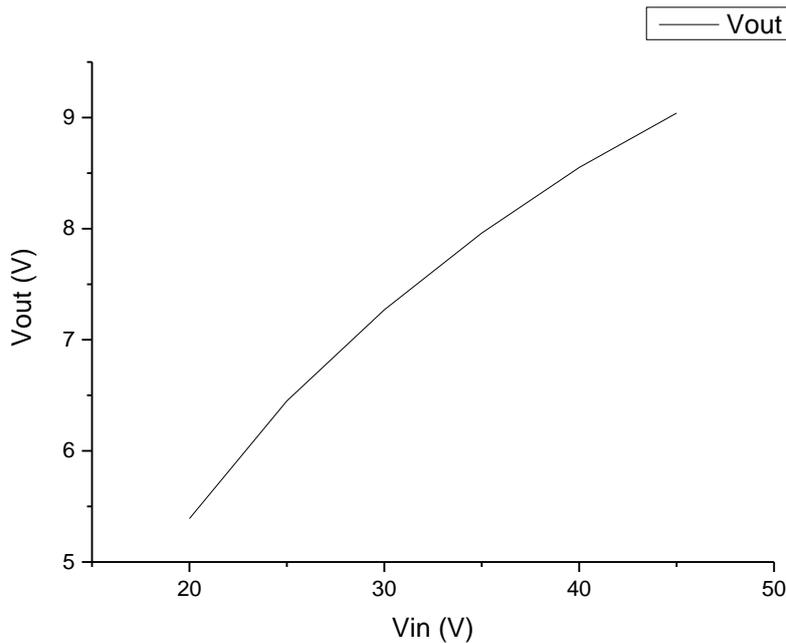


Fig 4.5 Relationship between input voltage and output voltage  
when duty cycle 33.33%

#### 4.2.2 When the input voltage is certain, change the duty cycle

Assuming input voltage is 40V, the period of ePWM is 100 $\mu$ s, and the duty cycle of ePWM1 and ePWM2 both are 50%, just to change the duty cycle of ePWM3 and ePWM4 to get the corresponding output voltage. The setting of duty cycle of ePWM3 and ePWM4 is illustrated as table 4.2. The table 4.3 and figure 4.6 shows the relationship between duty cycle and output voltage when input voltage 40V.

Table 4.2 The setting of duty cycle of ePWM3 and ePWM4

Signals	Setting	Duty cycle (%)
ePWM3	2500	33.3
ePWM4	1250	
ePWM3	2250	40
ePWM4	1500	
ePWM3	2000	46.67
ePWM4	1750	

Table 4.3 The relationship between duty cycle and output voltage (input 40V)

<b>Duty cycle (%)</b>	33.33	40	46.67
<b>Output voltage (V)</b>	8.5	10.8	12.6

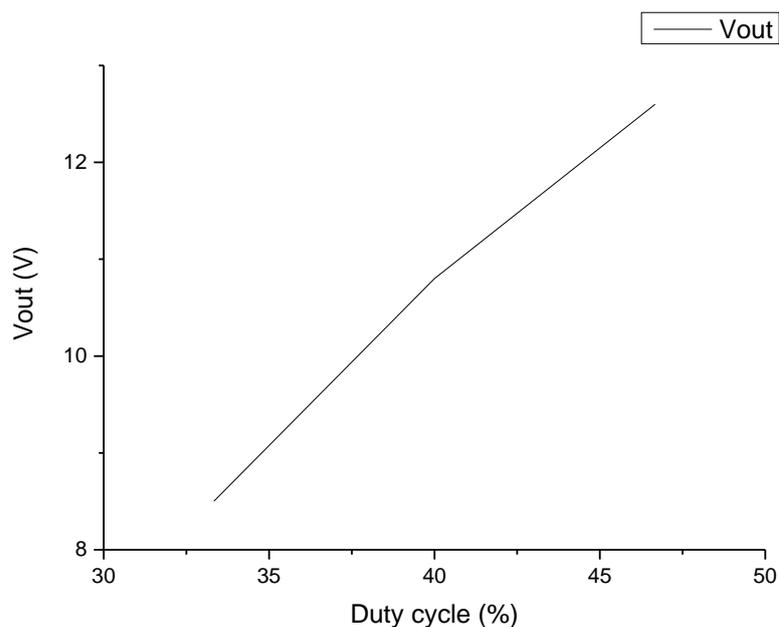
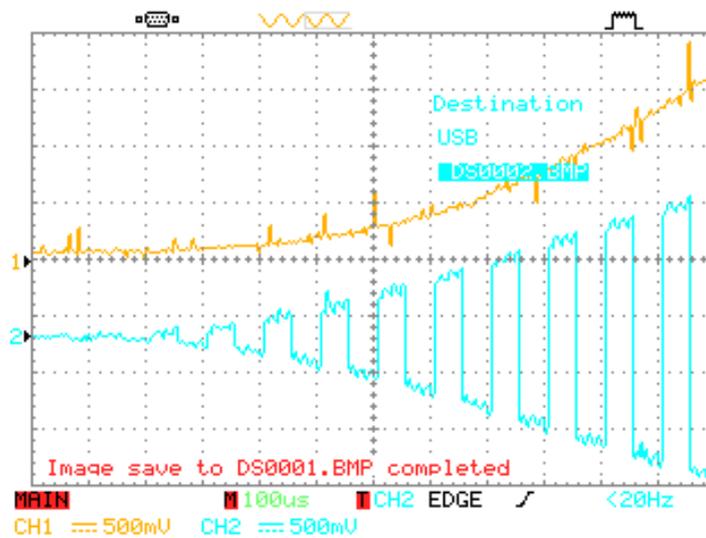


Fig 4.6 Relationship between duty cycle and output voltage (input 40V)

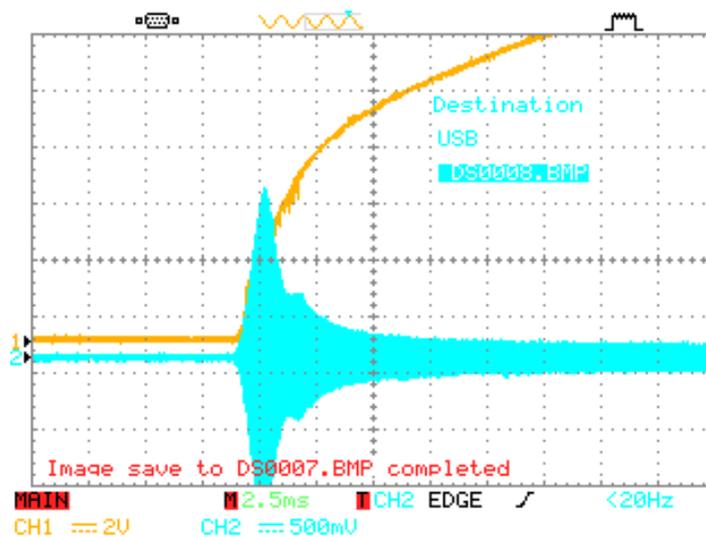
### 4.3 Power stage with feedback

The general idea of the feedback system is testing the current through the primary winding of transformer. The current is captured through a small

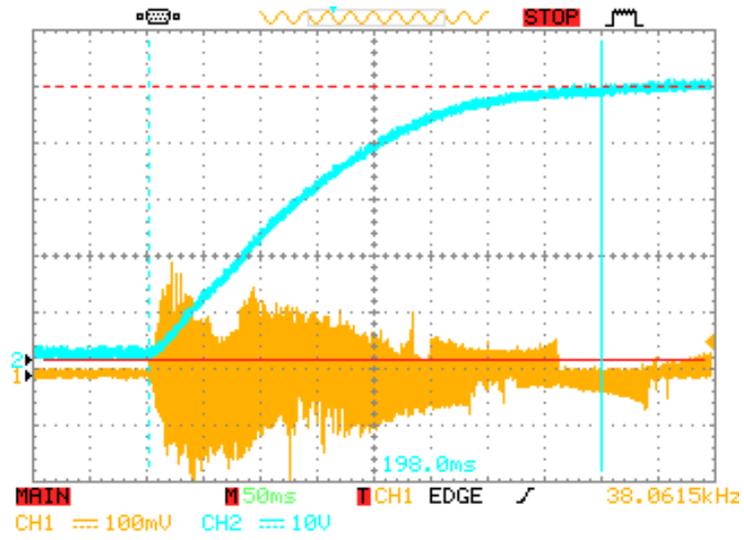
transformer to a AC current, then is converted by a full bridge to a DC voltage. Such voltage will go through ADC model of CPU to form a digital signal that is performed by a compare block so that an error signal can come out. After processed by the PI regular, new PWM signals with adjustable duty cycle to control the lower switches will form to make the system to output more ideal voltage. The rising time of the voltage across the storage capacitor will be shown as the figure 4.7.



a. the duration of beginning 1milliseconds



b. the system without feedback



c. the system with feedback

Fig. 4.7 The rising time of voltage across the storage capacitor

## CHAPTER 5: CONCLUSION

As the data and error of the result are in the believable range, the project and the experiment can be treated as true, and the corresponding analysis of information can be meaningful. According to data captured and analyzed above, the following conclusions can be gotten:

1. When is input voltage is certain, if the duty cycle of the lower transistor s(Q3 and Q4) increases, the output voltage will grows;
2. When the duty cycle is certain, the growing input voltage leads the increasing output voltages;
3. When the circuit adds feedback system, the adjustable duty cycle of PWM leads a stable output voltage;
4. The voltage across storage capacitor in the rising time turns a linear growing when the feedback system added.

What's more, when the transistors to be switched on or off, the pulse and obvious ripples of voltage between the collector and emitter pins of transistors, between the base and emitter pins of transistor and transformer Tr1 will come out. But the snubber circuit will absorb certain current to eliminate the effect.

In a summary, the power supply device can produce a stable and controllable output voltage.

## REFERENCE

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